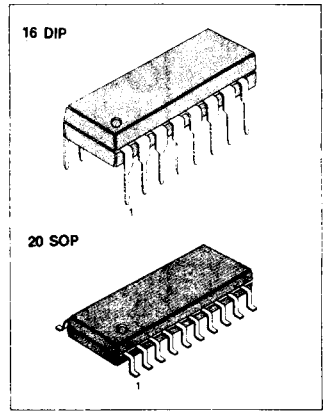
16-BIT D/A CONVERTER FOR CDPs

The KDA0316 is a CMOS, 16-bit digital-to-analog converter for compact disc players that uses a dynamic level shift conversion method, combining R-string, Pulse Width Modulation and level shift.



FEATURES

- **2's complement serial data input**
- **Contains two-channel D/A converter**
- **Can output L out and R out in phase**
- **To 176.4kHz maximum sampling frequency (corresponding to four oversampling)**
- **No deglich circuit needed**
- **Si-gate CMOS process (low power consumption)**
- **Single 5V supply voltage**
- **Built-in test circuit for PWM DAC**
- **Output swing level can be adjusted by the V_R input voltage**
- **MSB first and LSB first mode of input digital audio data is available**

APPLICATIONS

- Portable cassette radios with CDP
- Home audio component systems
- Electronic keyboards
- Music centers
- Mini CDPs
- Car CDPs

ORDERING INFORMATION

Device	THD(Max)(%)	Package	Operating Temperature
KDA0316LN	0.05	20 DIP	−30°C ~ +75°C
KDA0316N	0.08		
KDA0316LD	0.05	20 SOP	
KDA0316D	0.08		

PIN CONFIGURATION

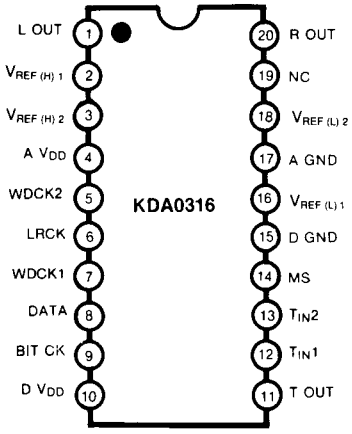


Fig. 1

PIN DESCRIPTION

Pin No	Symbol	Description
1	L OUT	Left channel output pin
2	$V_{REF\ (H)\ 1}$	Top reference voltage 1 pin
3	$V_{REF\ (H)\ 2}$	Top reference voltage 2 pin
4	A V_{DD}	Analog supply voltage pin
5	WDCK2	Word clock 2 input pin
6	LRCK	Left/right clock input pin
7	WDCK1	Word clock 1 input pin
8	DATA	Digital audio data input pin
9	BIT CK	Bit clock input pin
10	D V_{DD}	Digital supply voltage pin
11	T OUT	Test output pin
12	$T_{IN}1$	Test input pin
13	$T_{IN}2$	Test input pin
14	MS	Mode selecting pin
15	D GND	Digital ground pin
16	$V_{REF\ (L)\ 1}$	Bottom reference voltage 1 pin
17	A GND	Analog ground pin
18	$V_{REF\ (L)\ 2}$	Bottom reference voltage 2 pin
19	NC	No connection
20	R OUT	Right channel output pin

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	$-0.3 \sim +7.0$	V
Input Voltage	V_I	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage	V_O	$-0.3 \sim V_{DD}+0.3$	V
Operating Temperature Range	V_{OPR}	$-30 \sim +75$	°C
Storage Temperature Range	V_{STG}	$-40 \sim +125$	°C
ESD Susceptibility (Note 3)	V_{ESD}	±900	V
Latch-up Current	I_{LATCH}	50	mA

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Operating Temperature Range	T_{OPR}	−30		75	°C
Input High Voltage	V_{IH}	2.2		$V_{DD}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Reference High Voltage	$V_{REF\,(L)}$	$V_{DD}-0.5$		V_{DD}	V
Reference Low Voltage	$V_{REF\,(H)}$	0		0.5	V
Sampling Frequency	f_S			176.4	KHz

ELECTRICAL CHARACTERISTICS

(Converter Specifications: $V_{DD}=5V$, $V_{REF\,(H)}=5V$, $V_{REF\,(L)}=$ A GND, IF = 0V, $f_S=176.4KHz$, Ta = 25°C., unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	$V_{DD}=5V$		3.5	5.5	mA
		$V_{DD}=5.5V$		4.0	7.0	
Total Harmonic Distortion	THD	MS = 0V or 5V Data = 1KHz, 0dB			0.05*1 0.08	%
		MS = 0V or 5V Data = 1KHz, −20dB			0.2	
Signal to Noise Ratio	S/N	Data = 1KHz, 0dB		92		dB
		$V_{DD}=4.5V$ Data = 1KHz, 0dB		87		
		MS = 5V Data = 1KHz, 0dB		92		
		MS = 5V, $V_{DD}=4.5V$ Data = 1KHz, 0dB		87		
Crosstalk	CT	Data = 1KHz, 0dB		−85		dB

*1: User's option value (KDA016LN, KDA0316LD)

Note 1: ABSOLUTE MAXIMUM RATINGS are those values beyond which the life of the device may be impaired. Normal operation is not guaranteed at these extremes.

Note 2: All voltage is measured with respect to the GND, unless otherwise noted. The separate A GND point should always be wired to the D GND.

Note 3: The 100pF is discharged through a 1.5KΩ resistor.

(2) V_{DD} and V_R power supply should be low impedance and high stable (for example, a three-terminal voltage

TEST CIRCUIT

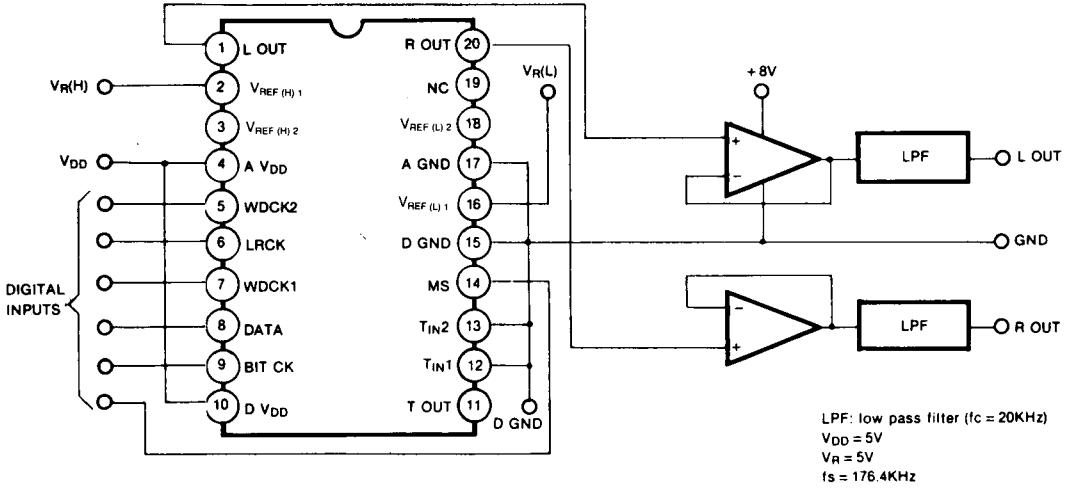
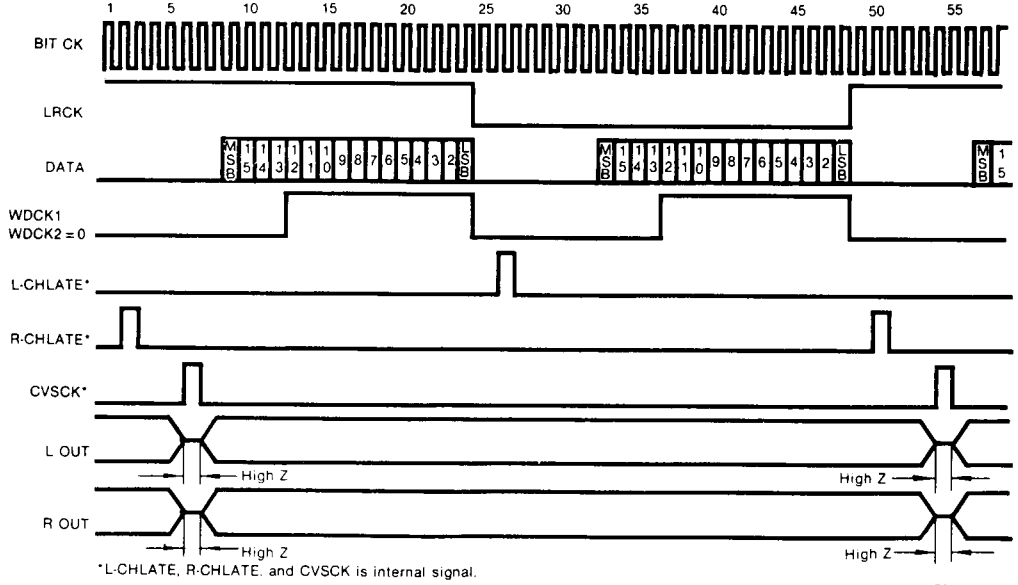


Fig. 2

APPLICATION INFORMATION

TIMING DIAGRAM 1 (When MS = "H")

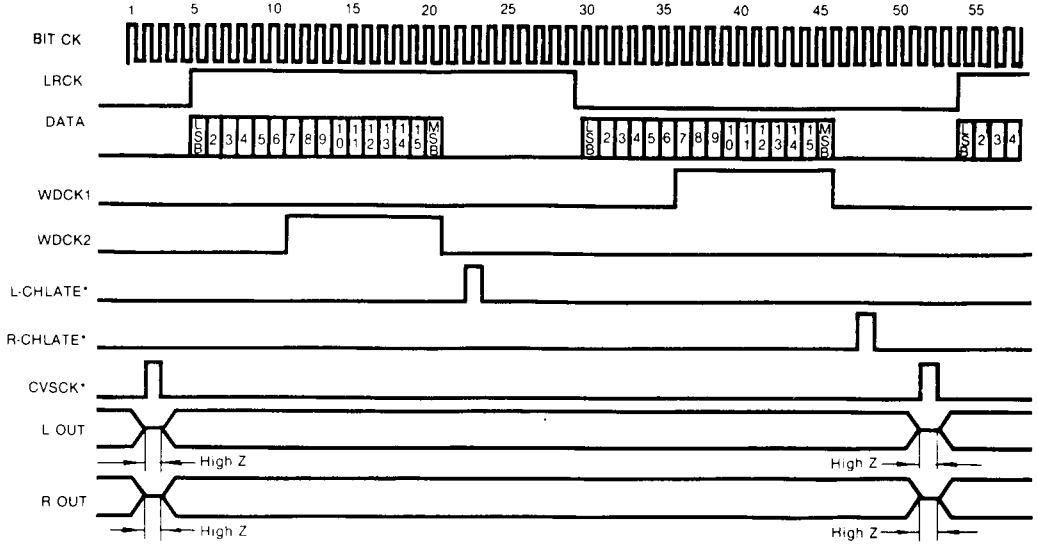


*L-CHLATE, R-CHLATE, and CVSCK is internal signal.

Fig. 3

BIT CK = 8.4672MHz (f_S = 176.4KHz)
4.2336MHz (f_S = 88.2KHz)
2.1168MHz (f_S = 44.1KHz)

TIMING DIAGRAM 2 (When MS = "L")



*L-CHLATE, R-CHLATE, and CVSCK is internal signal.

Fig. 4

BIT CK = 8.6436MHz (f_S = 176.4KHz)
4.3218MHz (f_S = 88.2KHz)
2.1609MHz (f_S = 44.1KHz)

APPLICATION CIRCUIT

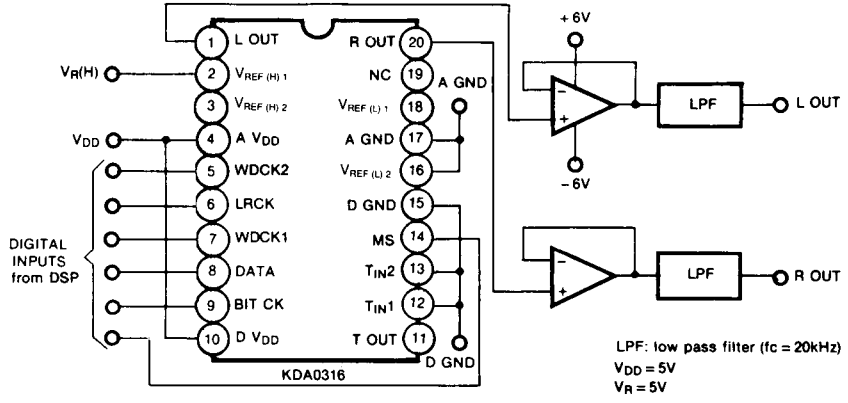


Fig. 5

Note: (1) D GND should be wired to the digital ground group and A GND to the analog ground group.
(2) V_{DD} and V_R power supply should be low impedance and high stable (for example, three-terminal voltage regulator).
(3) Because of the low output impedance and weak noise immunity of Pin 1 or Pin 20, noise reduction should be done by reducing the lead-wire length to the next OP amp stage.